ABSTRACT OF DISCLOSURE

The bus selector device 3 is arranged independent of the master chip 1 and substantially at the same distance from the master chip 1 and the slave chips 2a to 2c. In the transmission of data and commands, the master chip 1 outputs a connection information signal indicating the connection of the buses B and Ba to Bc among the chips 1 and 2a to 2c to the bus selector device 3. Based on the connection information signal, the bus selector device 3 switches and selects among the bus connections of the chips 1 and 2a to 2c. Consequently, the buses among the chips 1 and 2a to 2c have an equal and short length, realizing a high-speed data transmission among these chips. In addition, the number of pins in the master chip 1 can be reduced.